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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,835	03/30/2004	Kazuaki Goto	030712-29	3051

22204 7590 04/12/2006

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EXAMINER	
ROSSOSHEK, YELENA	
ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/811,835	GOTO ET AL.	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9-15* is/are rejected.

7)☒ Claim(s) *8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/30/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/811,835 filed 03/30/2004.

2. Claims 1-15 are pending in the Application.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

4. The abstract of the disclosure is objected to because page 7 has an typographical error on the line 2: "grater" needs to be replaced by –greater--; moreover, for accuracy the term "greater" has to be replaced with term –less--

Correction is required. See MPEP § 608.01(b).

Claim Objections

5. Claims 2-5, 7-9, 11-15 are objected to because of the following informalities:

first indefinite article "A" has to be replaced by –The-- to avoid insufficient antecedent basis for the claims 2-5, 7-9, 11-15

claim 5 line 8 delete "anther" insert –another--

claim 15 line 8 delete "anther" insert –another--

claim 8 is formulated unclear to what Applicant intent to mean, particularly, it is not clear in which area logic cells are deleted (last limitation), since it was not claimed before any appearance of the logic cells in the spare underground cell area.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-7, 9-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Solomon et al. (US Patent 6,446,248).

With respect to claim 1 Solomon et al. teaches a method of designing a circuit layout of a semiconductor integrated circuit (abstract), comprising: designing a logic function of the integrated circuit within inserting a standard cells as shown on the Fig. 4 (col. 7, ll.20-21), wherein during integrated circuit design standard cells are pre-designed and configured to perform a predetermined function (col. 4, ll.64-65); designing a pattern layout of the integrated circuit so that the pattern layout includes a logic cell area and an open area as shown on the Fig. 4, wherein integrated circuit layout includes logic cells (standard cells) to determine the function of the integrated circuit and unused areas (open) 401, 402, 403, 404, 405, 406 (col. 7, ll.19-21); inserting a spare underground cell into the open area within inserting revision or spare cells as extra cells (col. 3, ll.43-45), wherein spare cells are inserted into unused by standard cells areas (open) (col. 4, ll., 28-31), wherein the spare underground cell includes a functional element within revision cells as a collection of logic gates, buffers or memory elements (col. 3, ll.46-47); and designing a mask layout of the integrated circuit,

the mask layout including the logic cell and the spare underground cell within creating the layout of the integrated circuit by inserting standard cells and spare cells by forming ponds of gates (POGs) with further creating the mask for the integrated circuit (col. 4, ll.33-37).

With respect to clam 6 Solomon et al. teaches a method of changing a circuit layout of a semiconductor integrated circuit within a method for designing integrated circuit and making a changes to the design when is desired by modifying spare cells (col. 4, ll.33-37), comprising: preparing the circuit layout including a logic cell area and a spare underground cell area within inserting standard cells into the layout of the integrated circuit (col. 4, ll.21-22), wherein standard cells are pre-designed to perform predetermined function (logic) (col. 4, ll.64-65) and then inserting spare (base) cells on the unused space in the integrated circuit layout (col. 4, ll.24-26; ll. 62-63), wherein the spare underground cell area includes a functional element within base cells containing transistors (functional elements) having unconnected terminals (col. 5, ll.10-13); hypothetically disposing a changing layout into the spare underground cell area within inserting the functionally uncommitted base cells having unconnected terminals (col. 5, ll.10-13); preparing a list of the changing layout by determining unused area 401-406 after standard cells have been inserted into the layout as shown on the Fig. 4 (col. 7, ll.19-21); deciding the position of the changing layout by extracting the unused areas 401-406 using area-based placement routing tool (col. 7, ll.21-22); and automatically setting a conductive pattern layout of the semiconductor integrated circuit and using area-based placement routing tool for

placing ponds of gates (POGs) 411-416 as shown on the Fig. 4A (col. 7, ll.25-26), wherein POGs are sets of base cells (spare) (col. 7, ll.28-29).

With respect to claim 10 Solomon et al. teaches a method of designing a circuit layout of a semiconductor integrated circuit (abstract), comprising: designing a logic function of the integrated circuit within inserting a standard cells as shown on the Fig. 4 (col. 7, ll.20-21), wherein during integrated circuit design standard cells are pre-designed and configured to perform a predetermined function (col. 4, ll.64-65); designing a pattern layout of the integrated circuit so as to include a plurality of logic cells in a logic cell area and an open area within inserting standard cells into the layout of the integrated circuit (col. 4, ll.21-22), wherein standard cells are pre-designed to perform predetermined function (logic) (col. 4, ll.64-65) and then inserting spare (base) cells on the unused space in the integrated circuit layout (col. 4, ll.24-26; ll. 62-63), wherein the spare underground cell area includes a functional element within base cells containing transistors (functional elements) having unconnected terminals (col. 5, ll.10-13); inserting a plurality of spare underground cells into the open area within inserting revision or spare cells as extra cells (col. 3, ll.43-45), wherein spare cells are inserted into unused by standard cells areas (open) (col. 4, ll., 28-31), wherein each of the spare underground cells includes a plurality of functional elements within revision cells as a collection of logic gates, buffers or memory elements (col. 3, ll.46-47); and designing a mask layout of the integrated circuit, the mask layout including the logic cells and the spare underground cells within creating the layout of the integrated circuit by inserting standard cells and spare cells by

forming ponds of gates (POGs) with further creating the mask for the integrated circuit (col. 4, ll.33-37).

With respect to claims 2-5, 7, 9, 11-15 Solomon et al. teaches:

Claims 2, 7, 11: wherein the functional element includes a D flip-flop, an inverter, a NOR circuit, a NAND circuit an exclusive OR circuit and a latch circuit (col. 5, ll.14-16);

Claims 3, 13: wherein inserting the spare underground cell includes: dividing the pattern layout into a plurality of block regions within partitioning the layout of the integrated circuit into blocks as shown on the Fig. 4 (col. 2, ll.50-51); searching the open area from the block regions by searching and extracting empty spaces, i.e. unused by standard cells (col. 4, ll.23-24); distributing the open area into the block regions (col. 7, ll.21-22); and inserting the spare underground cell into the distributed open area using area-based placement routing tool for placing ponds of gates (POGs) 411-416 as shown on the Fig. 4A (col. 7, ll.25-26), wherein POGs are sets of base cells (spare) (col. 7, ll.28-29);

Claims 4, 14: wherein the inserting the spare underground cell into the distributed open area includes: pointing out an open area in an attended block region and an attended spare underground cell within the area-based placement/routing tool for extracting the unused (open) areas 401-406 as shown on the Fig. 4 (col. 7, ll.21-23); inserting the attended spare underground cell into the open area in the attended block region using area-based placement routing tool for placing ponds of gates (POGs) 411-416 as shown on the Fig. 4A (col. 7, ll.25-26), wherein POGs are sets of base cells (spare) (col. 7, ll.28-29); renewing

the attended block region as shown on the Fig. 4A, wherein new layout is depicted after inserting POGs 411-416; and setting a flag when all inserting within the attended block region are finished by setting the limit of the size of POGs according of the size of each unused area (open), wherein the number of the transistors contained in each POG depends on the size of each POG (col. 7, ll.35-37);

Claims 5, 15: wherein the inserting the spare underground cell into the distributed open area further includes: renewing the attended spare underground cell by forming desired spare cells according to the desired design changes (col. 4, ll.30-31); and repeating the pointing out, the inserting the attended spare underground cell, renewing the attended block region, setting and renewing the attended spare underground cell with another open area in another attended block region and another attended spare underground cell until all of the block regions are finished within performing floorplanning and placement after partitioning the layout, wherein placement is done in a iterative mode, such as performing an initial placement and then performing iterative improvements until the layout has minimum optimum area corresponding to the design specification (col. 3, ll.5-9);

Claim 9: further comprising designing a mask of the semiconductor integrated circuit after the setting within creating the layout of the integrated circuit by inserting standard cells and spare cells by forming ponds of gates (POGs) with further creating the mask for the integrated circuit (col. 4, ll.33-37);

Claim 12: wherein each of the spare underground cells has a same kind of the functional elements (col. 5, ll.14-16).

Allowable Subject Matter

8. Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Also claim 8 has to be modified with clarification according the claims objection above. The prior art of record does not teach replacing a logic cell in the circuit layout with a spare underground cells.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner
Helen Rossoshek
AU 2825

PAUL DINH
PRIMARY EXAMINER